

**Notice of Allowability**

Application No.

09/540,614

Examiner

Syed Zia

Applicant(s)

GRAWROCK, DAVID W.

Art Unit

2131

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 01/06/2006.
2. ☒ The allowed claim(s) is/are 1,2,4,6-10,12-15 and 17-22.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some\* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date \_\_\_\_\_
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_



## **DETAILED ACTION**

### ***Response to Amendment***

This office action is in response to amendment and argument filed on January 06, 2006. Original application contained Claims 1-23. Applicant previously amended Claim 1, 9, 14, and 18. Applicant currently amended Claim 1, 6, 9, 14 and 18. The amendments filed on January 06, 2006 have been entered and made of record. Therefore, presently Claims 1-23 are pending for consideration, and Examiner's amendment is based on this currently recorded claims (dated January 06, 2006).

## **EXAMINER'S AMENDMENT**

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with William W. Schaal (Reg. No: 39,018) on Thursday February 23, 2006.

This application has been amended as follows:

IN THE CLAIMS

Cancel Claims 3, 5, 11, 16, and 23 without prejudice.

Replace Claims 1-2, 4, 6-10, 12-15, and 17-22 as follows:

1. A method comprising:

implementing an integrated circuit device within an electronic system, the integrated circuit device including a control storage element, an override disable pin and an override pin which, when asserted, allows a stored representation of a primary pass-phrase to be modified; and

preventing modification of a representation of the primary pass-phrase when the override disable pin is asserted by (i) setting the control storage element within the integrated circuit device upon assertion of the override disable pin and (ii) disabling modification of the primary pass-phrase when the control storage element is set, the primary pass-phrase permitting access to stored information within a non-volatile memory of the integrated circuit device implemented within the electronic system when the primary pass-phrase is input by the user and the primary pass-phrase is determined to be correct based on a comparison conducted between a value computed from the primary pass-phrase and the representation of the primary pass-phrase.

2. The method of claim 1, wherein the integrated circuit device comprises a package to form a packaged integrated circuit device.

4. The method of claim 1, wherein the control storage element is set after placing the electronic system in an administration mode upon correctly inputting the primary pass-phase into the electronic system.

6. The method of claim 1, wherein the preventing of the modification of the primary pass-phase includes signaling a control application software initiating a request for modification of the pass-phase that a user is denied access to the stored information of the integrated circuit device unless the primary pass-phase is correctly entered and prohibiting modification of the representation of the primary pass-phase.

7. The method of claim 1, wherein the representation of the primary pass-phase includes a hash value of the primary pass-phase.

8. The method of claim 1, wherein control storage element includes at least one control register configured for permanent state retention over a plurality of power cycles.

9. A method comprising:  
enabling access to stored information within an electronic system, the information including a representation of a primary pass-phase, upon assertion of an override pin of an integrated circuit device; and

disabling access to the stored information despite assertion of the override pin of the integrated circuit device when the integrated circuit device is powered on and an override disable pin of the integrated circuit device is asserted prior to assertion of the override pin unless the primary pass-phase is correctly supplied by a determination using the representation of the primary pass-phase, the disabling of access comprises (i) setting a control storage element

within the integrated circuit device in response to the assertion of the override disable pin, and  
(ii) determining whether the control storage element is set.

10. The method of claim 9, wherein the integrated circuit device comprises a package to form a packaged integrated circuit device.

12. The method of claim 9, wherein the control storage element is set after placing the electronic system in an administration mode upon correctly inputting the primary pass-phrase into the electronic system.

13. The method of claim 9, wherein the setting of the control storage element includes setting a bit of at least one control register configured for permanent state retention over a plurality of power cycles.

14. A method comprising:  
enabling placement of an integrated circuit device of an electronic system into an administrator mode upon assertion of an override pin of the integrated circuit device, data stored within the integrated circuit device can be cleared only when the integrated circuit device is placed in the administrator mode; and

disabling placement of the integrated circuit device of the electronic system into the administrator mode despite assertion of the override pin of the integrated circuit device when an override disable pin of the integrated circuit device is asserted prior to assertion of the override pin so that the primary pass-phrase needs to be supplied before access to the data stored within the integrated circuit device is allowed, the disabling of access comprises (i) setting a control

storage element within the integrated circuit device in response to the assertion of the override disable pin, and (ii) determining whether the control storage element is set.

15. The method of claim 14, wherein the integrated circuit device comprises a package to form a packaged integrated circuit device.

17. The method of claim 14, wherein the setting of the control storage element includes setting a bit of at least one control register configured for permanent state retention over a plurality of power cycles.

18. An electronic system comprising:

a bus;

a processor coupled to the bus;

a system memory coupled to the bus; and

an integrated circuit device coupled to the bus, the integrated circuit device including:

an integrated circuit package,

a memory contained to the integrated circuit package,

an override pin of the integrated circuit package to enable access to and modification of a representation of a primary pass-phrase upon assertion of the override pin, the primary pass-phrase permitting access to information stored within the memory,

an override disable pin of the integrated circuit package to disable access to and modification of a representation of the primary pass-phrase despite the assertion of the override pin when the override disable pin is asserted prior to assertion of the override pin, and

a microcode to determine whether the override disable pin has been asserted prior to assertion of the override pin.

19. The electronic system of claim 18, wherein the integrated circuit further comprises a package to contain the memory from which the override pin and the override disable pin protrude.

20. The electronic system of claim 18, wherein the memory of the integrated circuit device is non-volatile memory.

21. The electronic system of claim 18, wherein the integrated circuit device further includes a control storage element.

22. The electronic system of claim 21, wherein the control storage element of the integrated circuit device includes at least one control register configured for permanent state retention over a plurality of power cycles.

*Allowable Subject Matter*

1. Claims 1-2, 4, 6-10, 12-15, and 17-22 are allowed.
2. The following is an Examiner's statement of reason for allowance:

The above mentioned claims are allowable over prior arts because the combined system of Cited Prior Art of record fails to teach or render obvious the claimed limitations in combination with the specific added limitations, as recited in independent Claims 1, 9, 14, 18, and subsequent dependent claims, when analyzed in light of specification.

In the system of cited prior arts with an output disable pin, when the indicator is set, the OVER-RIDE signal causes the powerdown controller to ignore any power-up commands from an external powerdown signal, and when the indicator has not been set, however, the OVER-RIDE signal does not cause powerdown controller to ignore a power-up command by providing access to stored information.

Therefore, the system combining the cited prior art does not suggest an operation of preventing modification of a representation of a primary pass-phrase, such as primary pass phrase itself, or derivation of the pass phrase, when the override disable pin is asserted. Hence, the system of cited prior art does not address the drawbacks of situations of existing art when the override disable pin is inserted and the user accidentally forget the pass-phrase, then the user is fully precluded from accessing the stored information that may render the device inoperable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed Zia whose telephone number is 571-272-3798. The examiner can normally be reached on 9:00 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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February 23, 2006

